CLAIMS

1. An off chip driver impedance adjustment circuit, comprising:

a storage circuit adapted to receive and store a drive strength adjustment word;

a counter circuit coupled to the storage circuit to receive the drive strength adjustment word and operable to develop a drive strength count responsive to the drive strength adjustment word, the counter circuit having a current value of the drive strength adjustment count set therein; and

an output driver circuit coupled to the counter circuit to receive the drive strength count and being adapted to receive a data signal, the driver circuit operable to develop an output signal on an output responsive to the data signal and adjust a drive strength as a function of the drive strength count.

2. The off chip driver impedance adjustment circuit of claim 1 wherein the counter circuit is set with a programmable value from a fuse code.

3. The off chip driver impedance adjustment circuit of claim 1 wherein the counter circuit increments or decrements the current value of the drive strength adjustment count responsive to the drive strength adjustment word to develop the drive strength adjustment count.

4. The off chip driver impedance adjustment circuit of claim 1 wherein the counter circuit comprises:

a pull-up counter circuit coupled to the storage circuit to receive selected bits of the stored drive strength adjustment word, and operable to develop a pull-up drive strength count responsive to the selected bits; and

a pull-down counter circuit coupled to the storage circuit to receive selected bits of the stored drive strength adjustment word, and operable to develop a pull-down drive strength count responsive to the selected bits .

5. The off chip driver impedance adjustment circuit of claim 4 wherein the output driver circuit comprises:

a first predriver circuit adapted to receive the data signal and the pull-up drive strength count from the pull-up counter circuit, the first predriver circuit operable to develop a pull-up drive strength word responsive to the pull-up drive strength count and the data signal; and

a second predriver circuit adapted to receive the data signal and the pull-down drive strength count from the pull-down counter circuit, the second predriver circuit operable to develop a pull-down drive strength word responsive to the pull-down drive strength count and the data signal.

6. The off chip driver impedance adjustment circuit of claim 5 wherein output driver circuit further comprises:

a pull-up driver circuit coupled to the first predriver circuit to receive the pull-up drive strength word and operable to adjust a pull-up drive strength of the output signal as a function of the pull-up drive strength word when the output signal is to be driven high; and

a pull-down driver circuit coupled to the second predriver circuit to receive the pull-down drive strength word and operable to adjust a pull-down drive strength of the output signal as a function of the pull-down drive strength word when the output signal is to be driven low.

7. The off chip driver impedance adjustment circuit of claim 6 wherein each of the pull-up and pull-down driver circuits comprises a plurality of transistors coupled between a voltage supply and an output node on which the output signal is developed, a control terminal of each transistor being coupled to receive a respective bit of the corresponding drive strength word.

8. The off chip drive impedance adjustment circuit of claim 5 wherein each of the predriver circuits further includes a resistive network that controls a slew rate of bits forming the drive strength word.

9. The off chip driver impedance adjustment circuit of claim 1 wherein the storage circuit comprises a latch.

10. The off chip driver impedance adjustment circuit of claim 1 wherein the output driver circuit is further operable to adjust the drive strength as a function of drive strength mode bits.

11. The off chip driver impedance adjustment circuit of claim 10 wherein the drive strength mode bits include a half drive strength bit and a default drive strength word.

12. A driver adjustment circuit, comprising:

a storage circuit coupled to a data bus;

a pull-up counter coupled to the storage circuit;

a pull-down counter coupled to the storage circuit;

a first predriver adapted to receive a data signal and coupled to the pull-up counter;

a second predriver adapted to receive the data signal and coupled to the pull-down counter;

a pull-up driver coupled to the first predriver and coupled to an output node; and

a pull-down driver coupled to the second predriver and coupled to the output node.

13. The driver adjustment circuit of claim 12 further comprising a write control circuit coupled to at least the storage circuit and the counters.

14. The driver adjustment circuit of claim 13 further comprising an extended mode register coupled to the write control circuit and the counters.

15. A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit;

an extended mode register; and

an off chip driver impedance adjustment circuit coupled to the memory-cell array and the control circuit, the circuit comprising:

a storage circuit coupled to the data bus to receive and store a drive strength adjustment word;

a counter circuit coupled to the storage circuit to receive the drive strength adjustment word and operable to develop a drive strength count responsive to the drive strength adjustment word, the counter circuit having a current value of the drive strength adjustment count set therein; and

an output driver circuit coupled to the counter circuit to receive the drive strength count and coupled to the data bus and the memory-cell array to receive a data signal, the driver circuit operable to develop an output signal on the data bus responsive to the data signal and adjust a drive strength as a function of the drive strength count.

16. The memory device of claim 15 wherein the counter circuit of the off chip driver impedance adjustment circuit of is set with a programmable value from a fuse code.

17. The memory device of claim 15 wherein the memory device comprises a DDR II SDRAM.

18. The memory device of claim 15 wherein the counter circuit increments or decrements the current value of the drive strength adjustment count responsive to the drive strength adjustment word to develop the drive strength adjustment count.

19. The memory device of claim 15 wherein the counter circuit comprises:

a pull-up counter circuit coupled to the storage circuit to receive selected bits of the stored drive strength adjustment word, and operable to develop a pull-up drive strength count responsive to the selected bits; and

a pull-down counter circuit coupled to the storage circuit to receive selected bits of the stored drive strength adjustment word, and operable to develop a pull-down drive strength count responsive to the selected bits .

20. The memory device of claim 19 wherein the output driver circuit comprises:

a first predriver circuit adapted to receive the data signal and the pull-up drive strength count from the pull-up counter circuit, the first predriver circuit operable to develop a pull-up drive strength word responsive to the pull-up drive strength count and the data signal; and

a second predriver circuit adapted to receive the data signal and the pull-down drive strength count from the pull-down counter circuit, the second predriver circuit operable to develop a pull-down drive strength word responsive to the pull-down drive strength count and the data signal.

21. The memory device of claim 20 wherein output driver circuit further comprises:

a pull-up driver circuit coupled to the first predriver circuit to receive the pull-up drive strength word and operable to adjust a pull-up drive strength of the output signal as a function of the pull-up drive strength word when the output signal is to be driven high; and

a pull-down driver circuit coupled to the second predriver circuit to receive the pull-down drive strength word and operable to adjust a pull-down drive strength of the output signal as a function of the pull-down drive strength word when the output signal is to be driven low.

22. The memory device of claim 21 wherein each of the pull-up and pull-down driver circuits comprises a plurality of transistors coupled between a voltage supply and an output node on which the output signal is developed, a control terminal of each transistor being coupled to receive a respective bit of the corresponding drive strength word.

23. The memory device of claim 20 wherein each of the predriver circuits further includes a resistive network that controls a slew rate of bits forming the drive strength word.

24. The memory device of claim 20 wherein the output driver circuit is further operable to adjust the drive strength as a function of drive strength mode bits stored the extended mode register.

25. The memory device of claim 24 wherein the drive strength mode bits include a half drive strength bit and a default drive strength word.

26. A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit;

an extended mode register; and

an off chip driver impedance adjustment circuit coupled to the memory-cell array and the control circuit, the circuit comprising:

a storage circuit coupled to the data bus to receive and store a drive strength adjustment word;

a counter circuit coupled to the storage circuit to receive the drive strength adjustment word and operable to develop a drive strength count responsive to the drive strength adjustment word, the counter circuit having current value of the drive strength adjustment count set therein; and

an output driver circuit coupled to the counter circuit to receive the drive strength count and coupled to the data bus and the memory-cell array to receive a data signal, the driver circuit operable to develop an output signal on the data bus responsive to the data signal and adjust a drive strength as a function of the drive strength count.

27. The computer system of claim 26 wherein the counter circuit of the off chip driver impedance adjustment circuit of is set with a programmable value from a fuse code.

28. The computer system of claim 26 wherein the memory device comprises a DDR II SDRAM.

29. The computer system of claim 26 wherein the counter circuit increments or decrements the current value of the drive strength adjustment count responsive to the drive strength adjustment word to develop the drive strength adjustment count.

30. The computer system of claim 26 wherein each of the predriver circuits further includes a resistive network that controls a slew rate of bits forming the drive strength word.

31. The computer system of claim 26 wherein the output driver circuit is further operable to adjust the drive strength as a function of drive strength mode bits stored the extended mode register.

32. The computer system of claim 26 wherein the drive strength mode bits include a half drive strength bit and a default drive strength word.

33. A method of adjusting a drive strength of an output driver, the method comprising:

setting a drive strength count;

storing a drive strength adjustment word;

adjusting the drive strength count as a function of the drive strength adjustment word; and

adjusting the drive strength of the output driver as a function of the drive strength count.

34. The method of claim 33 wherein setting the drive strength count comprises presetting the drive strength count to a value programmed by a programmable fuse code.

35. The method of claim 33 wherein the drive strength adjustment word comprises a four bit word.

36. The method of claim 33 wherein adjusting the drive strength count as a function of the drive strength adjustment word comprises incrementing or decrementing an initial value of the count responsive the drive strength adjustment word.

37. The method of claim 33 wherein adjusting the drive strength of the output drive as a function of the drive strength adjustment word comprising adjusting an impedance between an output node and a supply voltage source and between the output node and a reference voltage source responsive to the drive strength adjustment word.

38. A method of adjusting a drive strength of an output driver in a memory device, the method comprising:

storing a drive strength adjustment word;

storing drive mode bits;

adjusting a drive strength count as a function of the drive strength adjustment word; and

adjusting the drive strength of the output driver as a function of the drive strength adjustment word and the drive strength bits.

39. The method of claim 38 wherein the drive mode bits comprise a half drive strength bit and a default drive strength word.

40. The method of claim 38 wherein adjusting the drive strength count as a function of the drive strength adjustment word comprises incrementing or decrementing an initial value of the count responsive the drive strength adjustment word.

41. The method of claim 38 wherein adjusting the drive strength of the output drive as a function of the drive strength adjustment word comprising adjusting an impedance between an output node and a supply voltage source and between the output node and a reference voltage source responsive to the drive strength adjustment word.

42. An off chip driver impedance adjustment circuit, comprising:

means for receiving and storing a drive strength adjustment word;

means for generating a drive strength count responsive to the drive strength adjustment word and a fuse code; and

means for driving an output signal on an output responsive to a data signal and for adjusting a drive strength of the output signal as a function of the drive strength count.

43. The off chip driver impedance adjustment circuit of claim 42 wherein the means for generating a drive strength count responsive to the drive strength adjustment word comprises means for incrementing or decrementing a current value of the drive strength adjustment count responsive to the drive strength adjustment word to develop the drive strength adjustment count.

44. The off chip driver impedance adjustment circuit of claim 42 wherein the means for generating a drive strength count comprises:

means for developing a pull-up drive strength count responsive to the selected bits of the stored drive strength adjustment word; and

means for developing a pull-down drive strength count responsive to the selected bits of the stored drive strength adjustment word.

45. The off chip driver impedance adjustment circuit of claim 44 wherein the means for driving comprises:

a first means for developing a pull-up drive strength word responsive to the pull-up drive strength count and the data signal; and

a second means for developing a pull-down drive strength word responsive to the pull-down drive strength count and the data signal.

46. The off chip driver impedance adjustment circuit of claim 45 wherein means for driving further comprises:

means for adjusting a pull-up drive strength of the output signal as a function of the pull-up drive strength word when the output signal is to be driven high; and

means for adjusting a pull-down drive strength of the output signal as a function of the pull-down drive strength word when the output signal is to be driven low.

47. The off chip driver impedance adjustment circuit of claim 42 wherein the means for driving is further operable to adjust the drive strength as a function of drive strength mode bits.

48. A driver adjustment circuit, comprising:

a predriver circuit configured to receive a strength code and a data signal and in response thereto generate a plurality of output driver control signals; and

an output driver circuit coupled to the predriver circuit to receive the plurality of output driver control signals, the output driver circuit operable to develop an output signal on an output node responsive to the data signal having a drive strength as a function of the plurality of output driver control signals.

49. The driver adjustment circuit of claim 48, further comprising a counter coupled to the predriver circuit, the counter having a programmable default value provided to the predriver circuit as the default strength code.

50. The driver adjustment circuit of claim 48 wherein the plurality of output driver control signals comprises a plurality of output driver control pull-up signals and a plurality of output driver control pull-down signals generated by the predriver circuit in response to the strength code and data signal.

51. The driver adjustment circuit of claim 50 wherein the output driver circuit comprises:

a pull-up driver circuit coupled to the predriver circuit to receive the plurality of output driver pull-up signals and operable to determine a pull-up drive strength of an output signal as a function of the plurality of output driver pull-up signals when the output signal is to be driven high; and

a pull-down driver circuit coupled to the predriver circuit to receive the plurality of output driver pull-down signals and operable to determine a pull-down drive strength of the output signal as a function of the plurality of output driver pull-down signals when the output signal is to be driven low.

52. The driver adjustment circuit of claim 51 wherein the strength code comprises a pull-up drive strength count and a pull-down drive strength count and the predriver circuit comprises:

a first predriver circuit adapted to receive the data signal and the pull-up drive strength count, the first predriver circuit operable to develop the plurality of output driver pull-up signals responsive to the pull-up drive strength count and the data signal; and

a second predriver circuit adapted to receive the data signal and the pull-down drive strength count, the second predriver circuit operable to develop the plurality of output driver pull-down signals responsive to the pull-down drive strength count and the data signal.